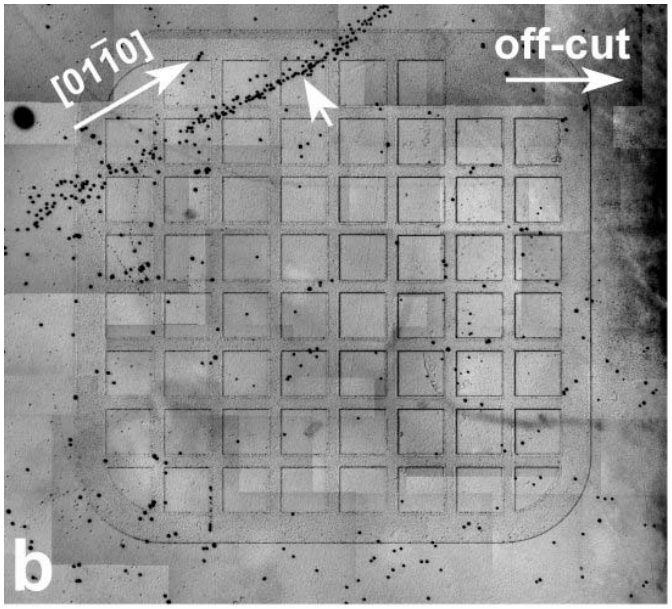
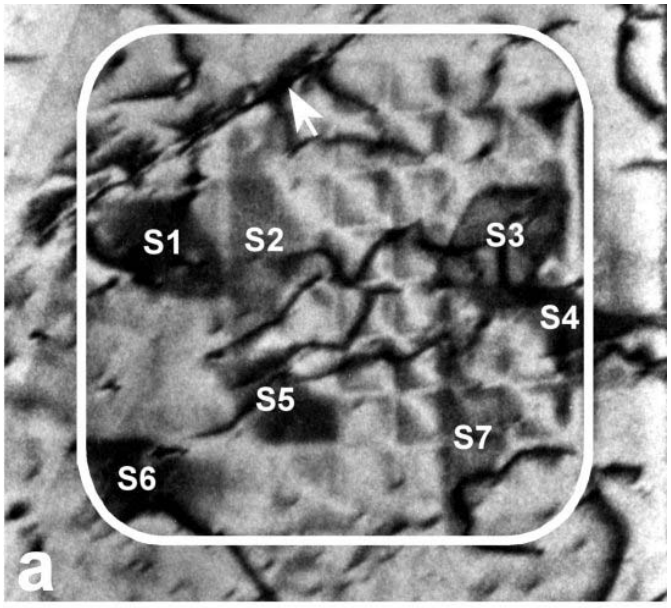

[01$\bar{1}$0]
off-cut
b
0.3 mm


S1
S2
S3
S4
S5
S6
S7
a
g=0$\bar{1}$10
0.3 mm

DMR-9903702

PI: M. Skowronski (GOALI project, in collaboration with SUNY Stony Brook, ABB and Cree)

Figure description

Upper figure shows an optical top view image of high voltage SiC diode with location of crystalline defects delineated by etching (dark dots). Diode area contains low angle grain boundary generated during growth of SiC wafer (row of pits in upper left corner) as well as other types of dislocations.

Lower figure is the transmission synchrotron white beam x-ray topograph of the same diode after electrical stress for 10 minutes and 1 Ampere. The dark diamond- and triangle-shaped areas correspond to stacking faults produced by current flow. The starting point for two of these defects (S1 and S2) are located at the low angle grain boundary.

Significance

The development of silicon carbide technology is driven by its potential applications in high voltage switching systems for efficient electric power distribution and electric vehicles. It was recently discovered that high voltage bipolar SiC devices severely degrade during current injection with degradation occurring through growth of stacking faults in SiC epilayers (shown in upper figure). Carnegie Mellon University together with ABB and Cree is working to produce stable and reliable SiC electronic devices. CMU work will identify the source of stress that causes fault expansion. Current hypothesis is the change of lattice parameter due to doping differences in p^+n^- structures. Also degradation can be prevented by identification and elimination of fault nucleation sites. One such site (low angle grain boundary in figures above) has been identified. Its origin is due to excessive temperature gradients during bulk crystal growth. Grain boundaries replicate from SiC wafers into epilayers during epitaxy. The solution is improved crystal growth with properly designed thermal gradients in the hot zone.